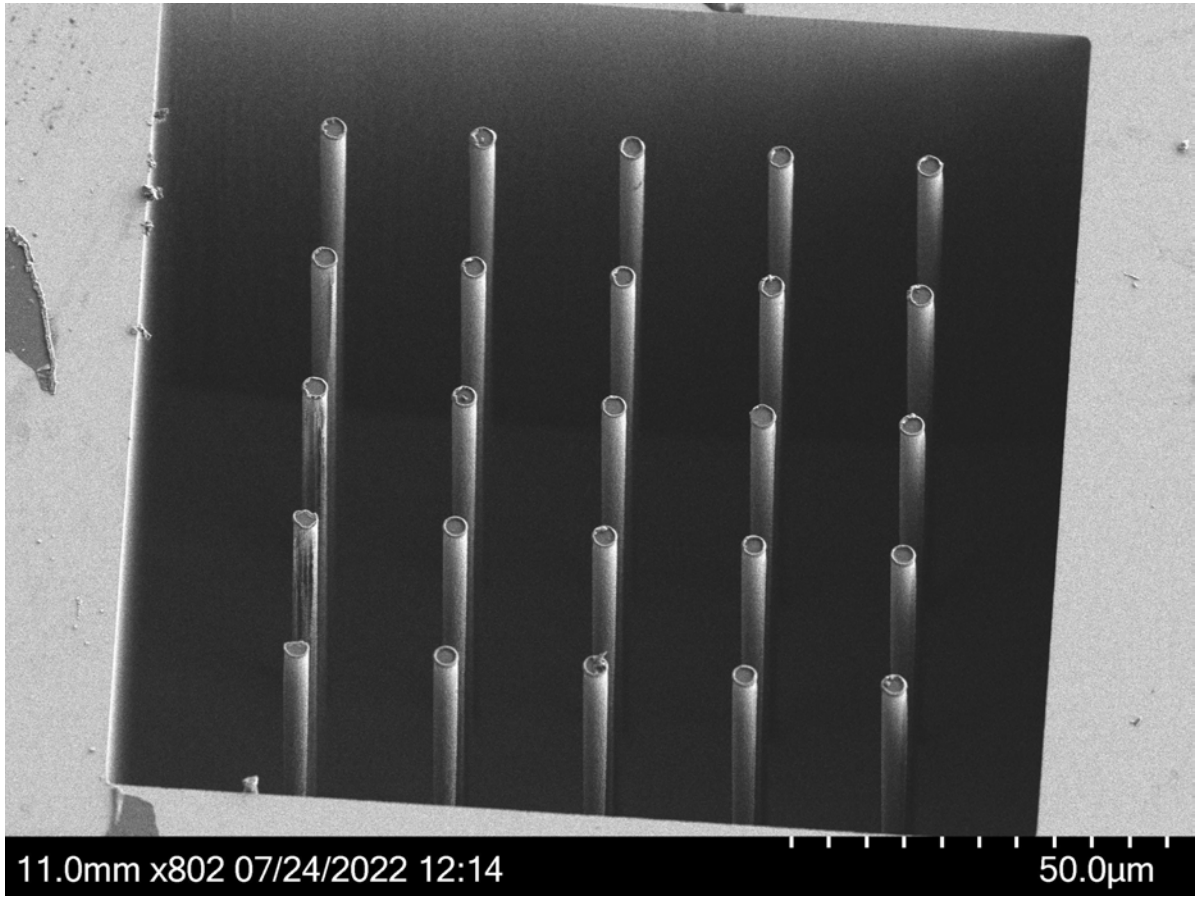
Fabrication of Silicon Micropillar Arrays Using the Bosch Process

David Li[1], Ling Xie[2], William Wilson[2]
[1]Lehigh University, [2]Harvard University,
NSF ECCS-2025158

Silicon micropillar arrays, which have applications in microfluidics, optoelectronics, and biosensing, are usually fabricated using photolithography and plasma etching. Photolithography selectively masks the silicon substrate with photoresist for etching. The silicon substrate is coated with photoresist, and selected parts of the photoresist are exposed to ultraviolet light to alter its solubility. The more soluble parts of the photoresist coating are then dissolved, leaving the pattern to be etched. The etching process consists of three main steps: polymer deposition to protect the sidewalls of the pillars, etching of the polymer at the floor of the array using ion bombardment, and etching of the silicon substrate. These steps enable pillars with a vertical profile to be formed. This process requires carefully controlled conditions in order to achieve the desired results, particularly if the pillars are small in diameter. Thus, we etched pillar arrays with varying conditions and examined them using a scanning electron microscope. In this way, we were able to optimize the etching conditions for pillars as small as one micron in diameter. We also discovered that with some of the etching conditions we studied, the etching process has an extremely high selectivity of well over 120:1 to the Microposit S1800 series photoresist and that the etch rate of silicon accelerates with depth; the two effects are inexplicable yet well-observed.



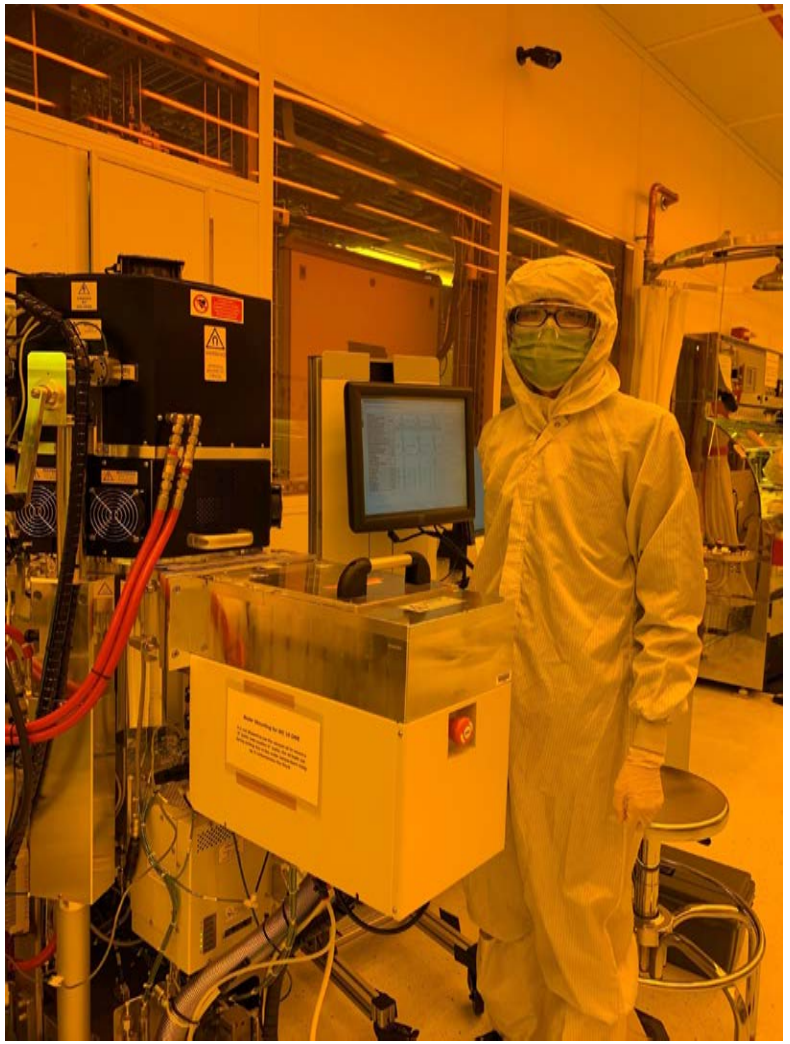
Array of silicon micropillars produced by etching.
Dimensions: 2 microns in radius, centers of the pillars separated by 20 microns, height approximately 180 microns

Fabrication of Silicon Micropillar Arrays Using the Bosch Process

David Li[1], Ling Xie[2], William Wilson[2]
[1]Lehigh University, [2]Harvard University,
NSF ECCS-2025158

David Li is a rising sophomore from Tucson, Arizona and attends Lehigh University in Bethlehem, Pennsylvania. He is majoring in electrical engineering and engineering physics. He intends to pursue a concentration in solid-state electronics and attend graduate school after graduation.

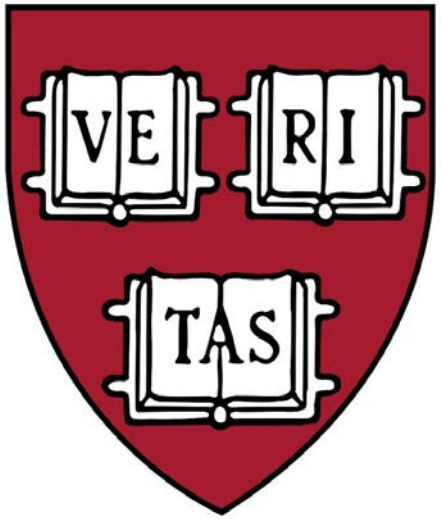
As I have only completed one year of my undergraduate studies, this is my first experience with producing original scientific research. I have learned so much about techniques used in microfabrication such as photolithography, dry etching, and scanning electron microscopy (SEM). In the process, I have also produced very intriguing, unexpected results from fabricating silicon micropillar arrays. I hope to apply the laboratory experience I have gained to electronic device research.



Using the SPTS Rapier DRIE to etch micropillar arrays.

Funding


NSF


VE
RI
TAS


National
Nanotechnology
Coordinated
Infrastructure


Center for
Nanoscale
Systems
Harvard University
FAS • SEAS